

Quantum device fine-tuning using unsupervised embedding learning

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Quantum devices with a large number of gate electrodes allow for precise control of device parameters. This capability is hard to fully exploit due to the complex dependence of these parameters on applied gate voltages. We experimentally demonstrate an algorithm capable of fine-tuning several device parameters at once. The algorithm acquires a measurement and assigns it a score using a variational auto-encoder. Gate voltage settings are set to optimise this score in real-time in an unsupervised fashion. We report fine-tuning times of a double quantum dot device within approximately 40 min.

I. INTRODUCTION

Electrostatically defined semiconductor quantum dots are intensively studied for solid-state quantum computation [1–4]. Gate electrodes in these device architectures are designed to separately control electrochemical potentials and tunnel barriers [5, 6]. However, these device parameters vary non-monotonically and not always predictably with applied gate voltages, making device tuning a complex and time consuming task. Fully automated device tuning will be essential for the scalability of semiconductor qubit circuits.

Tuning of electrostatically defined quantum dot devices can be divided into three stages. The first stage consists of setting gate voltages to create the confinement potential for electrons or holes. In our laboratory, full automation of this stage has been achieved as reported in Ref. [7]. The second stage, known as coarse tuning, focuses on identifying and navigating different operating regimes of a quantum dot device. Automated coarse tuning has been demonstrated using convolutional neural networks to identify the double quantum dot regime [8] and reach arbitrary charge states [9]. Template matching was also used to navigate to the single-electron regime [10]. During this stage, virtual gate electrodes can be used to independently control the electrochemical potential of each quantum dot [11, 12]. The third stage, referred to as fine-tuning, involves optimising a particular set of charge transitions. Previous work on automated fine-tuning focused on optimising the tunnel coupling between two quantum dots by systematically modifying gate voltages until this coupling converges to a target value [13, 14]. However, these approaches are restricted to a few device parameters and rely on calibration measurements.

Here, we demonstrate an automated approach for simultaneous fine-tuning of multiple device parameters, such as tunnel rates and inter-dot tunnel coupling. Our approach is based on a variational auto-encoder (VAE). In particu-

lar, we focus on double quantum dot devices. Electron transport through these devices is typically presented as a charge stability diagram, displaying the current flowing through the device as a function of two gate voltages. Bias triangles are regions in the stability diagram, for which current flow is allowed through a double quantum dot device under a bias voltage [15], and reveal most of the device parameters. Our algorithm aims at optimising various bias triangle characteristics commonly associated with favourable device parameters, as done by humans when tuning these devices. The VAE compresses training data displaying bias triangles to a lower-dimensional space, called the latent or embedding space. In this latent space, a human expert identifies target locations corresponding to bias triangles in the training set which exhibit favourable transport characteristics. The algorithm acquires a measurement displaying bias triangles and assigns to these bias triangles a location in latent space. The distance between this location and the chosen target locations is used by the algorithm as a basis to score the measurement, and this score is used to optimise the gate voltage settings in real time.

We have previously shown that VAEs significantly improve the efficiency of quantum dot measurements [16]. We have now, for the first time, used a VAE to fine-tune a double quantum dot device by locally optimising transport features in a completely automated manner. Without requiring any prior knowledge of the device architecture, we are able to fine-tune several device parameters at once.

II. DEVICE AND OVERVIEW OF THE ALGORITHM

We demonstrated our fine-tuning algorithm on a lithographically defined double quantum dot device. The device comprises a GaAs/AlGaAs heterostructure confining a two-dimensional electron gas (2DEG). Quantum dots

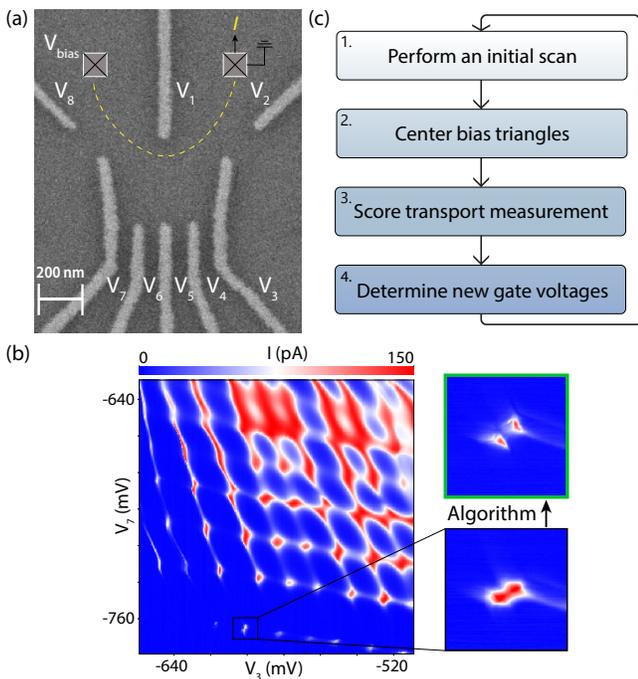


FIG. 1. Overview of the quantum dot device and algorithm. (a) Scanning electron microscopy image of a device lithographically identical to the one measured. A bias voltage V_{bias} is applied between two ohmic contacts to drive a current I through the device. Gate voltages V_1 to V_8 define and control the double quantum dot. (b) Current as a function of gate voltages V_3 and V_7 , with $V_{bias} = 0.2$ mV. In this stability diagram, at the cross-points of the hexagonal lattice representative of the double quantum dot regime, bias triangles are observed. The zoom in shows a pair of bias triangles that requires optimisation (bottom). This pair of bias triangles is displayed after optimisation (top), showing how the triangular shapes can now be distinguished. (c) Schematic overview of the fine-tuning algorithm. In each iteration an initial low resolution stability diagram displaying bias triangles is acquired (1). Subsequently, the bias triangles are centered in a gate voltage window using blob detection (2). In this window, the algorithm performs a high resolution measurement which is scored by the VAE (3). Based on the VAE score, the decision model proposes a new gate voltage configuration (4).

are defined by Ti/Au gate electrodes which are patterned on top of the heterostructure (Fig. 1a). DC voltages V_1 to V_8 are applied to these gate electrodes. A bias voltage V_{bias} determines the flow of current I through the device. A stability diagram for our double quantum dot device is shown in Fig. 1b. All measurements were performed at approximately 20 mK. The stability diagram exhibits bias triangles, which reveal device parameters such as charging energies, tunnel coupling to the left and right electrodes and inter-dot tunnel coupling. The shape, sharpness and brightness of bias triangles are related to those device parameters and are thus used to guide device tuning.

Our algorithm follows a similar approach to device tuning by humans. It consists of four major steps (Fig. 1c).

In each iteration, an initial low resolution stability diagram is acquired to center a pair of bias triangles. Next, a high resolution measurement of the bias triangles is performed and scored by the VAE. Based on this score, the set of gate voltages is determined for the next iteration.

III. VAE IMPLEMENTATION

The VAE consists of an encoder and decoder, both embodied in neural networks [17]. The encoder $q_\phi(\mathbf{z}|\mathbf{x})$ maps input data \mathbf{x} to a low-dimensional latent vector \mathbf{z} which is real-valued. The decoder $p_\theta(\mathbf{x}|\mathbf{z})$ maps a latent vector to a reconstruction $\hat{\mathbf{x}}$. The parameters of the encoder and the decoder neural networks are ϕ and θ , respectively. The VAE is a generative model; it seeks to preserve the maximum amount of information during the encoding process so that input data can be reconstructed with minimal error during the decoding process. During a training phase, ϕ and θ are iteratively updated to minimize a loss function. The loss function is given by a reconstruction error \mathcal{L}_{rec} , which penalises the networks for producing reconstructions that are dissimilar from the input data, and a regularisation term \mathcal{L}_{reg} , which enforces input data with similar characteristics to be encoded in close proximity in latent space. The reconstruction error and the regularisation term have weights α and β , respectively.

We implement Factor-VAE [18], an adaption of VAE that seeks to generate a latent space in which each dimension corresponds to a unique characteristic of the input data. The Factor-VAE framework assumes that there are underlying independent factors associated with the data. If fully disentangled, each of those factors can be identified with a dimension in latent space. By using a Factor-VAE, we aim to generate a latent space in which each dimension is associated with a single bias triangle characteristic, such as size or brightness. In this way, the distance in latent space to a target location results in a good metric to score acquired measurements.

The loss function of Factor-VAE includes a total correlation term which encourages the distribution of embeddings $q_\phi(\mathbf{z})$ to be disentangled. It is given by:

$$\mathcal{L}_{Factor-VAE} = \mathcal{L}_{rec} + \mathcal{L}_{reg} - \gamma D_{KL} \left(q_\phi(\mathbf{z}) \parallel \prod_j q_\phi(z_j) \right) \quad (1)$$

where the total correlation term is given by $D_{KL} \left(q_\phi(\mathbf{z}) \parallel \prod_j q_\phi(z_j) \right)$, i.e. the Kullback-Leibler divergence between the distribution of embeddings $q_\phi(\mathbf{z})$ and the product of the distribution of embedding components $\prod_j q_\phi(z_j)$, with the index j corresponding to the j th latent space dimension. The total correlation loss term has a weight γ . Since this term is intractable, it is estimated using a discriminator $D(\mathbf{z})$. The discriminator is trained to classify between non-factorial and factorial

samples, i.e. that its input is a sample from $q_\phi(\mathbf{z})$ rather than from $\prod_j q_\phi(z_j)$.

The training set for the Factor-VAE was collected from a device which differs considerably in material, architecture and transport regime from the device used to demonstrate the performance of the algorithm, evidencing its generality. The VAE was trained using 2253 sets of bias triangles, measured on a double quantum dot defined in a Ge/Si core-shell nanowire [19, 20]. In order to increase the robustness of the VAE, simple data augmentation techniques were applied. Data augmentation included translation, rotation, mirroring, Gaussian noise and random contrast, resulting in a total training set of 8732 stability diagrams of pixel resolution 32×32 . The dimension of the latent space was set to 10, as in Ref. [18], given the similar structure of input data. We tried multiple combinations of weights α , β and γ to achieve the optimal VAE performance, which was found empirically for $\alpha = 34$, $\beta = 1$ and $\gamma = 1$.

IV. SCORE METRIC

The score metric used by the algorithm is given by the distance between the latent space representation \mathbf{z} of an input stability diagram and the latent space representation $\{\tilde{\mathbf{z}}\}$ of a set of target inputs. Note that the loss function is used during training, while the score metric is used for optimisation. A measurement acquired by the algorithm is assigned a low (high) VAE score if its representation in latent space is near to (far from) the targets in latent space. Embeddings that are close together in latent space have similar \mathbf{z} , implying that the original inputs can be generated using similar underlying variables. As a result, bias triangles that are assigned a low score possess similar characteristics to the target bias triangles.

The target bias triangles are chosen from the unaugmented training set by a human expert who recognises in these triangles the characteristics indicative of favourable quantum dot parameters. The targets are augmented using the same augmentation techniques as described in III. Augmentation of 30 selected targets resulted in a total target set of size 360.

In Fig. 2 the latent space of the trained VAE is shown, and the embedding locations of example target and training inputs are indicated. A full plot of the latent space of the trained VAE with original input stability diagrams is shown in the Supplementary Material.

To write the expression for the score S_i , where i denotes the i th input measurement, we use the latent vector \mathbf{z}^i produced by the encoder for this measurement. The output of the encoder is assumed to follow a multivariate Gaussian with diagonal covariance structure: $q_\phi(\mathbf{z}|\mathbf{x}) = \mathcal{N}(\mathbf{z}; \boldsymbol{\mu}, \text{diag}(\boldsymbol{\sigma}^2))$, where the mean $\boldsymbol{\mu}$ and variance $\boldsymbol{\sigma}^2$ are outputs of the encoding network. Considering two independent normal distributions in latent space, the expectation value of the squared distance between the distributions is given by:

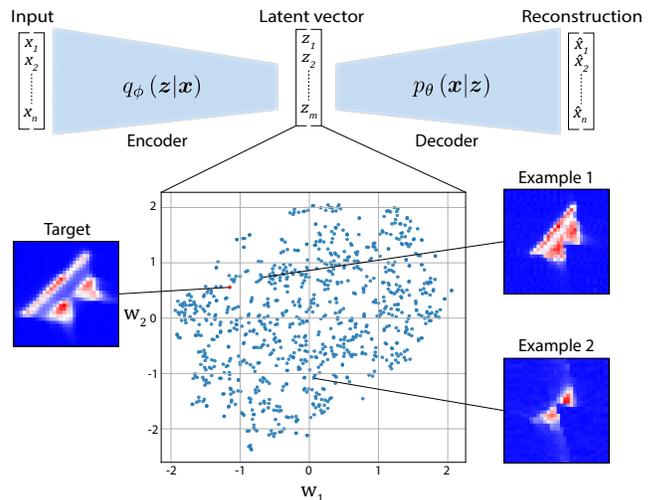


FIG. 2. Schematic overview of the VAE. The VAE consists of an encoder and decoder. The encoder $q_\phi(\mathbf{z}|\mathbf{x})$ compresses input stability diagrams to a lower-dimensional latent space. The decoder is denoted by $p_\theta(\mathbf{x}|\mathbf{z})$ and maps vectors in latent space \mathbf{z} to the distribution of input data. In this way, the input vector \mathbf{x} , for which each element is the brightness of one pixel in the stability diagram, is transformed into a reconstruction vector $\hat{\mathbf{x}}$. In order to visualise the ten-dimensional latent space, t-SNE is applied for dimensionality reduction [21]. The resultant two-dimensional latent space is described by a vector \mathbf{w} . Each dot represents the embedding of an input stability diagram. The embedding location of one of the target inputs is highlighted in red. It is expected that embeddings which are close to each other in latent space are generated by input data with similar characteristics. Test example 1, with similar characteristics to the target, can be found in close proximity to the target, whereas test example 2 is further away in latent space.

$$d(\mathbf{z}^1, \mathbf{z}^2) = \mathbb{E}(\|\mathbf{z}^1 - \mathbf{z}^2\|^2) = \|\boldsymbol{\mu}_{\mathbf{z}^1} - \boldsymbol{\mu}_{\mathbf{z}^2}\|^2 + \boldsymbol{\sigma}_{\mathbf{z}^1}^2 + \boldsymbol{\sigma}_{\mathbf{z}^2}^2 \quad (2)$$

For each input measurement embedded in latent space \mathbf{z}^i , (2) is used to determine the distance in latent space to target input $\tilde{\mathbf{z}}^j$. The final score S_i consists of the average of the distance to its k nearest targets:

$$S_i = \frac{1}{k} \sum_{\tilde{\mathbf{z}}^j \in A_k} d(\tilde{\mathbf{z}}^j, \mathbf{z}^i) \quad (3)$$

where A_k is the set of k targets closest to \mathbf{z}^i in latent space. In this way, optimal tuning corresponds to a low score. We found that for $k = 3$, the score metric produced a robust ranking of the training inputs in terms of their similarity to the targets.

V. OPTIMISATION

The optimisation starts from the device tuned to the double quantum dot regime so that at least one pair of bias triangles is identified, for which we used the algorithm presented in [7]. After acquiring the initial low resolution stability diagram, the bias triangles are centered using Laplacian of Gaussian (LoG) blob detection. In computer vision, blob detection techniques aim to detect bright regions on dark backgrounds or vice versa [22]. In Fig. 1b, the two examples of bias triangles displayed were centered with this novel approach. Once the triangles are centered, the high resolution scan (32×32 pixels, 17×17 mV) is acquired and evaluated using the VAE distance score metric. Based on the outcome value of S_i , a decision model sets the gate voltage configuration for the next stability diagram measurement. This process is iterated until the bias triangles are optimised in terms of characteristics such as shape, sharpness and brightness.

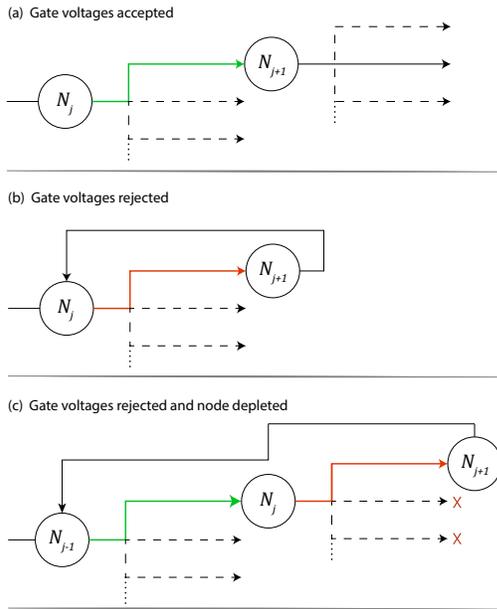


FIG. 3. Overview of the decision model. The set of applied gate voltages number j is indicated by N_j . The branched arrows represent the different gate voltage adjustment options, which are changes of $\pm\Delta V$ in every gate electrode to be tuned. In this figure, N_j represents the best scored gate voltage configuration obtained after a number of iterations. (a) Score S_i corresponding to a new configuration N_{j+1} is lower than at N_j , so the gate voltage change is accepted. For N_{j+1} , a new random gate voltage branch is selected and explored. (b) Score S_i corresponding to a new configuration N_{j+1} is higher than at N_j , so the gate voltage change is rejected. For N_j , one of the remaining gate voltage branches is randomly selected and explored. (c) If all possible gate voltage configurations are rejected the algorithm returns to the closest previously accepted gate voltage node that has unexplored branches. At this configuration, a gate voltage branch is randomly selected and explored.

The decision model for proposing gate voltage configurations is illustrated in Fig. 3. Node N_j represents the set of gate voltages $\{V_1^j, V_2^j, \dots, V_8^j\}$ applied by the algorithm. In each iteration, one gate electrode is selected at random, and the voltage applied to this electrode is modified by a fixed amount $\pm\Delta V$. Therefore, the algorithm chooses between a number of branches equal to twice the number of gate electrodes to be tuned. We chose $\Delta V = 2$ mV based on human experience in tuning similar devices. After centering and acquiring a high resolution measurement of the resulting bias triangles, the value of S_i determines the algorithm's decision. If S_i is lower than the previously best (lowest) scored bias triangles, the gate voltage change is accepted, leading to a new gate voltage configuration N_{j+1} . Conversely, if S_i is higher, the gate voltage change is rejected and the gate voltage setting returns to its previous configuration. In this case, the rejected gate voltage change will be an excluded branch in the random selection corresponding to the next iteration. Branches that lead to the reversal of the latest accepted gate voltage change are excluded too. It is possible that all gate voltage branches become depleted, in which case the decision model returns to the previously accepted gate voltage configuration with unexplored branches.

VI. EXPERIMENTAL DEMONSTRATION

We test the algorithm for different bias triangles measured on our device. Stability diagrams are measured as a function of barrier gate voltages V_3 and V_7 , which are adjusted during centering of the bias triangles. The gate voltages optimised by the algorithm are V_1 , V_2 and V_8 . For simplicity, we chose to keep gate voltages V_4 , V_5 and V_6 fixed. We checked their effect on the optimised bias triangles which were weak. All measured stability diagrams are min-max normalised with respect to the stability diagram obtained after the initial tuning to the double quantum dot regime. In Fig. 4, the optimisation of four different pair of bias triangles is shown.

In cases 1 to 3, the initial bias triangles lack a well-defined shape, indicative of small inter-dot tunnel coupling [15]. Furthermore, pronounced co-tunnelling lines, which are denotative of second-order transport processes, are observed. As the optimisation progresses, the bias triangles separate from each other and acquire a sharper triangular shape. Also, co-tunnelling currents are reduced. In the fourth case, the initial stability diagram shows very faint bias triangles. The optimisation algorithm proves capable of increasing the current flowing through the double quantum dot while preserving most of the other bias triangle characteristics. More examples of bias triangle optimisations achieved by our algorithm can be found in the Supplementary Material.

Fig. 5a shows S_i as a function of the number of iterations of our algorithm for cases 1 to 4. Most of the optimisation takes place during the first ten iterations, after which the score does not change significantly. In all

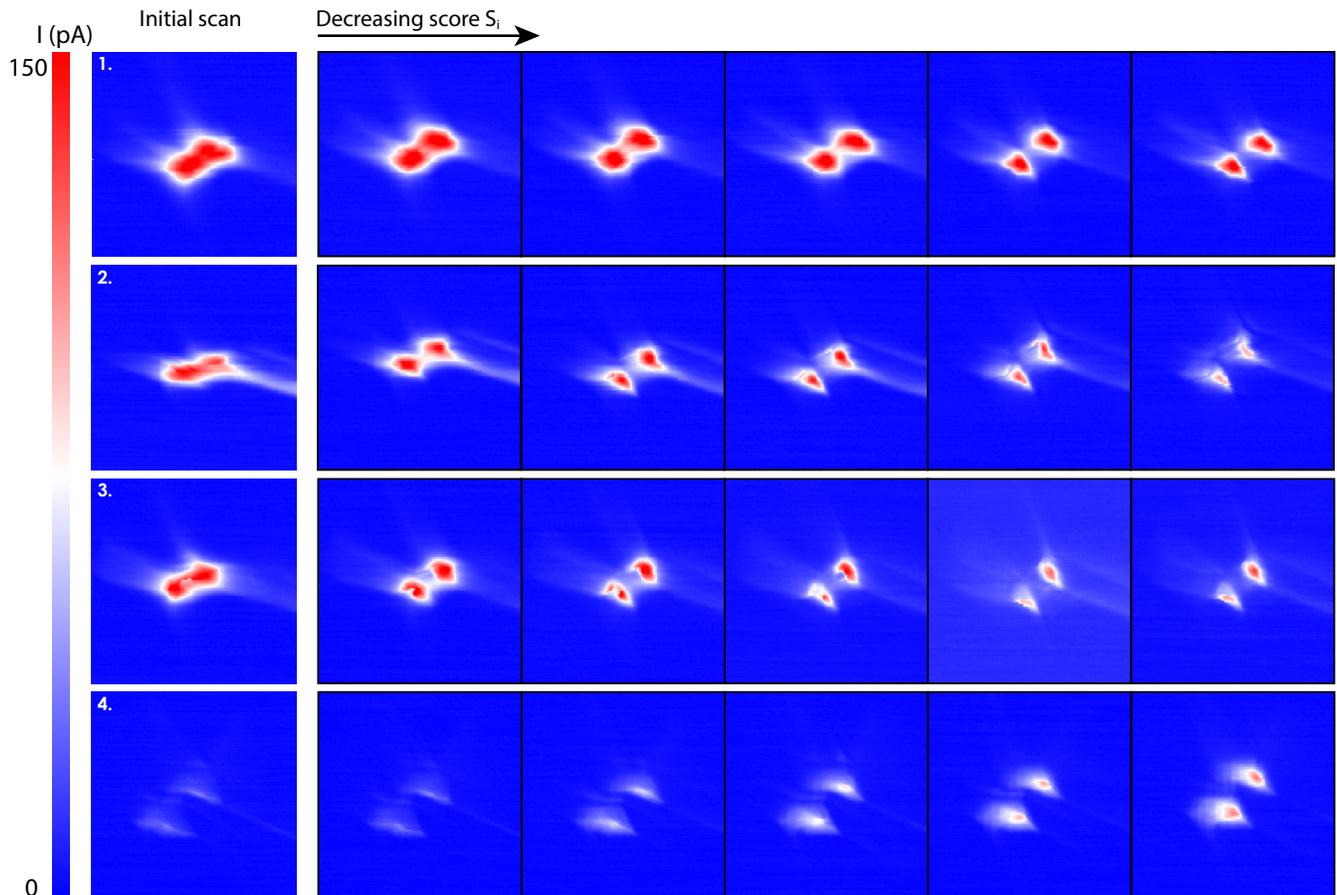


FIG. 4. Experimental demonstration of the algorithm. The first column shows four different pairs of bias triangles before the algorithm was run. Each row displays each of these bias triangles at selected iterations of the algorithm. For all these iterations, the applied gate voltage change led to a decrease in score S_i . All measurements were performed with $V_{bias} = 0.2$ mV. The stability diagrams were measured as a function of barrier gates V_3 and V_7 , while gate voltages V_1 , V_2 and V_8 were tuned by the algorithm.

cases, the algorithm completes the optimisation within 26 iterations, corresponding to a total tuning time of 36 min. This time is limited by the measurement time, which could be drastically reduced by radio-frequency reflectometry techniques [23–30].

In Fig. 5b we plot the trajectories in gate voltage space corresponding to each optimisation case. The average distance in gate voltage space between the initial gate voltage configurations is greater than for the final gate voltage configurations. This suggests that there exists a region in gate voltage space for which the bias triangles exhibit the most favourable transport characteristics, regardless of their values of V_3 and V_7 . Additional data can be found in the Supplementary Material.

VII. CONCLUSION

We experimentally demonstrate an optimisation algorithm for the fine-tuning of bias triangles in gate-defined quantum dots. The algorithm scores real-time measure-

ments by computing distances in the embedding space of a VAE. We show that this score can be used to locally optimise double quantum dot parameters in a completely automated manner. No prior knowledge of the device is required and the algorithm proves capable of tuning multiple device parameters at once.

The robustness and efficiency of the decision model could potentially be improved by using Bayesian optimisation or reinforcement learning for proposing new voltage configurations and minimising the score. Also, while we utilised the Euclidean distance between two Gaussian distributions for computing scores, recent work argues that the decoder induces a Riemannian metric in the latent space [31]. This would imply that shortest paths in latent space do not correspond to straight lines. Therefore, it might prove insightful to implement a Riemannian metric to measure latent space distances. Finally, the influence of selecting targets with different characteristics, such as different excited state energies, could be investigated in the future.

While all measurements presented are performed on

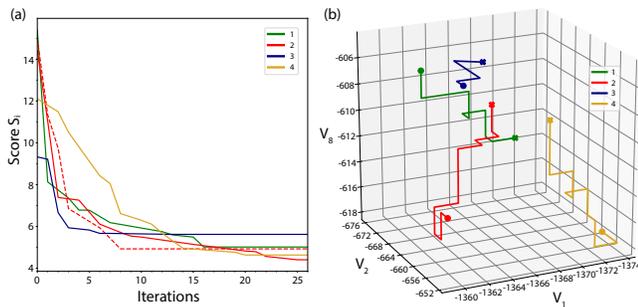


FIG. 5. Score S_i and gate voltage space trajectories during fine-tuning. (a) Score S_i as a function of the number of iterations of the optimisation algorithm. Solid lines 1 to 4 correspond to the optimisation cases presented in Fig. 4. The dashed line represents a different run of the algorithm for case 2. (b) Gate voltage space trajectories for the optimisation cases in Fig. 4. The starting (final) gate voltage configuration is denoted by a circle (cross).

a gate-defined GaAs double quantum dot, the VAE was trained on data obtained from a Ge/Si core-shell nanowire device, showing the algorithm is readily applicable to

different types of devices. Moreover, our algorithm can be adapted to include any number of additional gate electrodes, paving the way for the tuning of quantum dot arrays.

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SUPPLEMENTARY MATERIAL

A. Latent space

A representation of the latent space of the trained VAE with the bias triangles corresponding to each embedding is shown in Fig. S1.

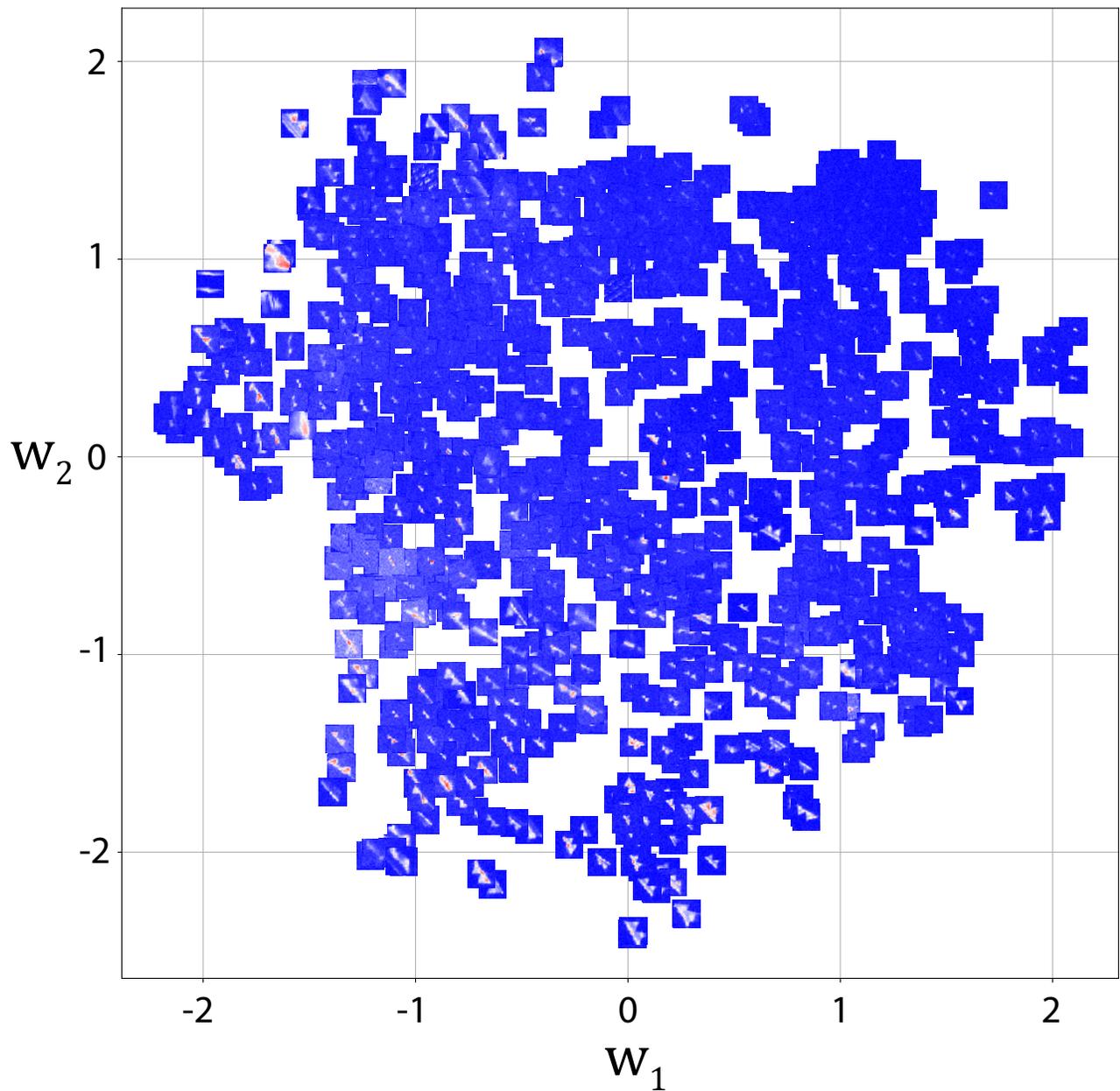


FIG. S1. Latent space of the trained VAE. In order to visualise the ten-dimensional latent embeddings, t-SNE [21] is applied for dimensionality reduction. The new two-dimensional latent space is described by a vector w . The original training inputs are plotted at the embedding locations.

B. Optimisation

The optimisation of different pairs of bias triangles is shown in Fig. S2 (cases S1 to S8) and Fig. S3 (cases S9 and S10). The stability diagrams correspond to gate voltage configurations for which a decrease in score S_i is observed. Fig. S4 presents the VAE score S_i as a function of the number of iterations of the optimisation algorithm for the optimisation cases in Fig. S2 and Fig. S3. The total gate voltage changes during fine-tuning are presented in Table S1.

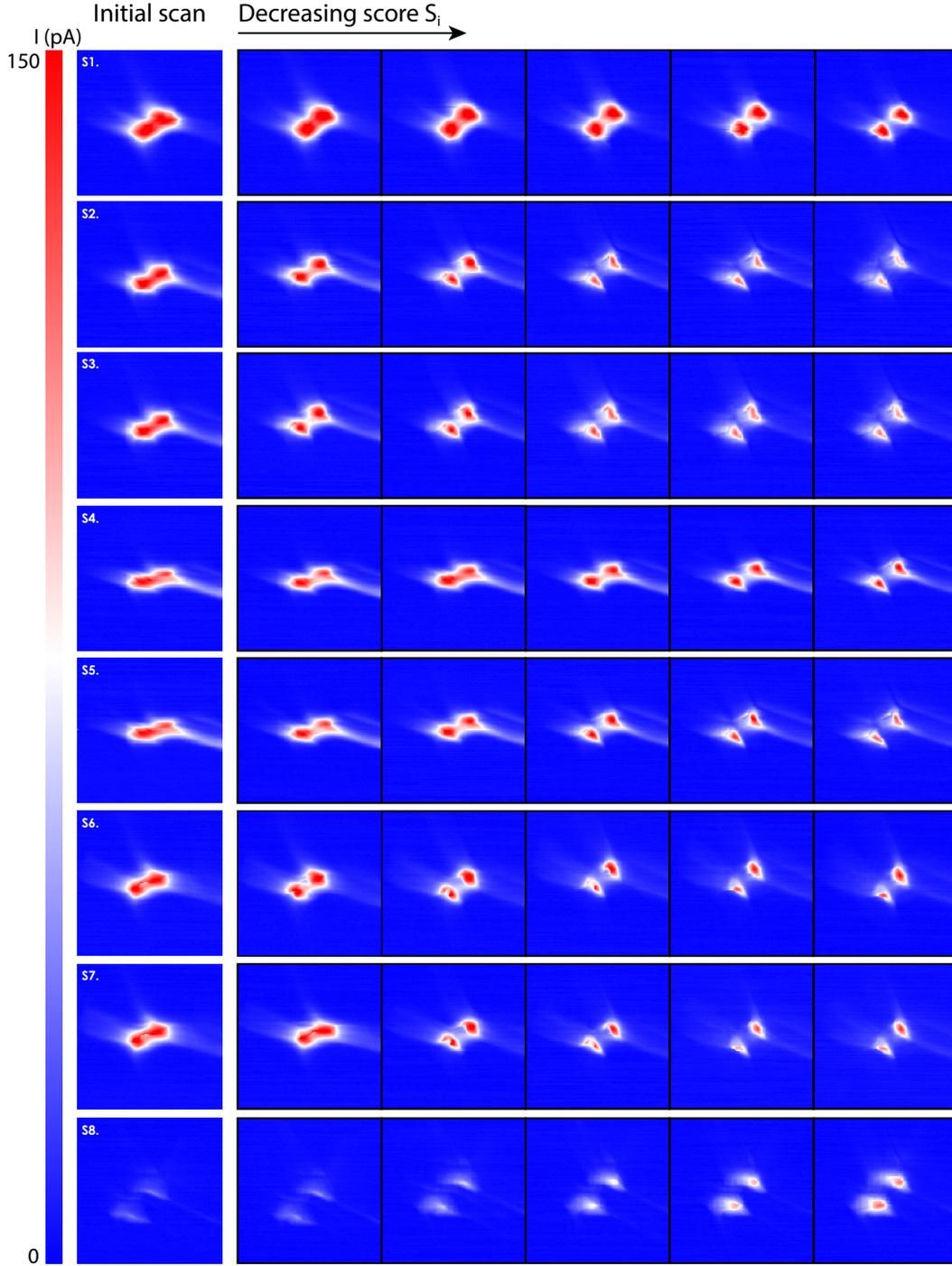


FIG. S2. Stability diagrams of bias triangles at different iterations of the optimisation algorithm. The stability diagrams correspond to iterations for which the gate voltage configuration led to a decrease in score S_i . Only a selection of the bias triangle measurements at accepted gate voltage configurations are plotted.

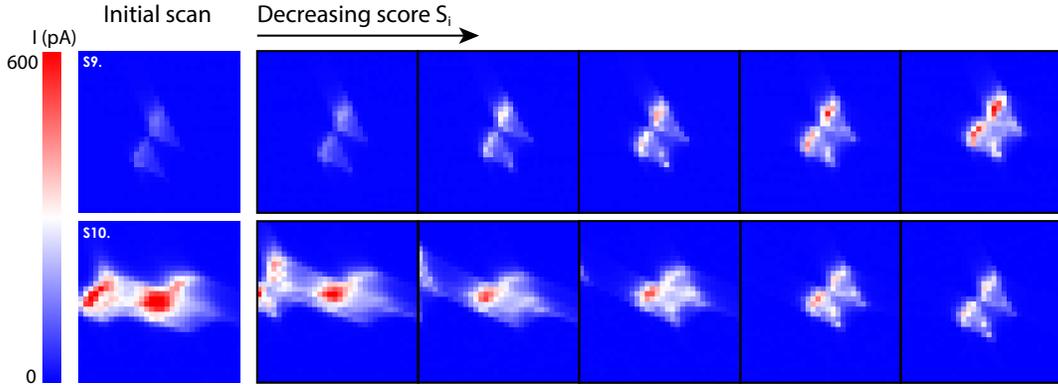


FIG. S3. Stability diagrams of bias triangles at different iterations of the optimisation algorithm. The stability diagrams correspond to iterations for which the gate voltage configuration led to a decrease in score S_i . Only a selection of the bias triangle measurements at accepted gate voltage configurations are plotted.

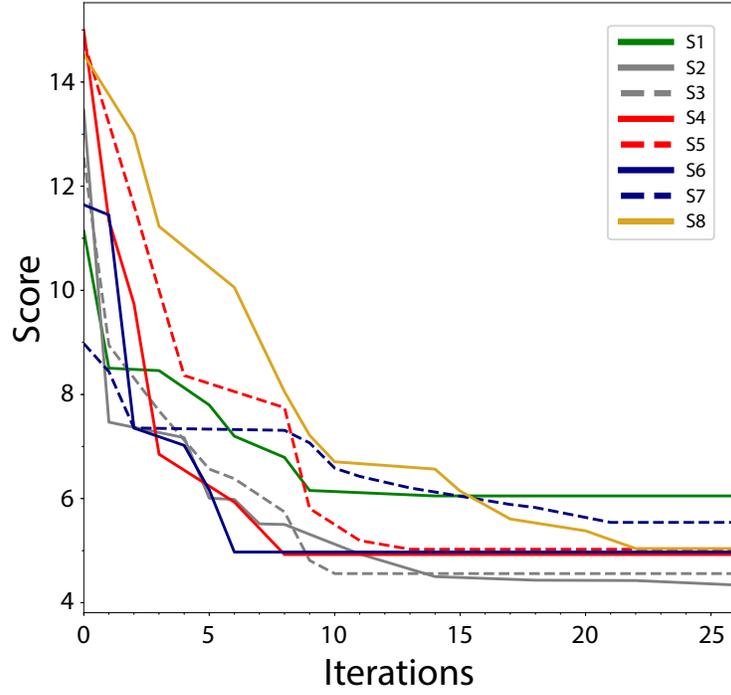


FIG. S4. Score S_i as a function of the number of iterations of the optimisation algorithm. The indexed lines correspond to the optimisation cases presented in Fig. S2. Dashed lines of the same colour represent different runs of the optimisation algorithm for given cases.

TABLE S1. Total gate voltage change (mV) during fine-tuning. Gates voltages V_1 , V_2 and V_8 were optimised, whereas gates V_3 and V_7 were used to center the bias triangles.

Case	ΔV_1	ΔV_2	ΔV_3	ΔV_7	ΔV_8
1	-8.0	0	6.29	5.92	-6.0
2	-6.0	-8.0	6.57	0	6.0
3	-4.0	-8.0	5.26	1.97	0
4	6.0	4.0	-3.94	-7.89	10.0
S1	-10.0	0	5.26	4.60	0
S2	-4.0	-10.0	5.92	1.31	0
S3	0	-8.0	2.63	0	-2.0
S4	-6.0	-2.0	3.94	1.97	2.0
S5	-4.0	-6.0	4.60	0.66	2.0
S6	0	-8.0	3.29	-1.31	2.0
S7	-2.0	-8.0	3.94	0.66	0
S8	14.0	0	-7.23	-9.86	4.0